PowerPC™

Upgrading PowerPC 601™ Evaluation Boards to Support the Intel® SIO 82378ZB

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PowerPC 601 evaluation boards that use the 82378IB SIO can be upgraded to use the 82378ZB.

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1 Overview

The first release of the PowerPC 601 evaluation board implements the Intel® SIO 82378IB chip (IB) as the PCI to ISA bridge. This document provides system designers with a suggested implementation using the Intel SIO 82378ZB part (ZB) that is now available.

In this document, *SIGNAL_NAMES* are denoted in italics, and `PIN_NAMES` are denoted in a different font.

For further information, refer to the PowerPC 601 User's Guide, the Intel SIO 82378IB/ZB data book, and the PowerPC 601 Design Kit I/O Interface EPLD Specification.

2 Arbitration

The ZB arbiter adds support for two additional PCI devices. This arbiter is not required in the PowerPC 601 evaluation board. The ZB arbiter must be disabled in the same way as the IB arbiter by driving `CPUREQ#` low during active `PCIRST#`.

3 Power Management

The new power management features of the ZB are not required in PowerPC 601 evaluation board.

4 Registers

There are several new registers on the ZB. Also, some of the current registers have changed definition. NO TAG is a list of the new and modified registers and their addresses:

Table 1. ZB Registers

Register Type	Address Offset (Hex)
New Configuration Registers	43h, 60h–63h, A0h–AEh
Modified Configuration Registers	08h, 40h, 42h, 56h
New ISA Registers	00B2h, 00B3h, 04D0h, 04D1h
Modified ISA Registers	20h,A0h

5 Interrupts

The major impact of the functional differences between the IB and ZB parts is in the handling of interrupts from the PCI slots.

5.1 Initial PowerPC 601 Evaluation Board Implementation Using the IB

The first releases of the PowerPC 601 evaluation board use the IB chip. As shown in NO TAG, the PCI interrupts from the PCI slots are shared with ISA interrupts and are assigned as follows:

- On the riser card, the four PCI interrupts (A,B,C,D) from each PCI slot are dot-ORed into a single interrupt line. For PCI slot1 this line is called *IRQ9#* and for PCI slot2 it is called *IRQ11#*.
- The interrupt from PCI slot1 *(IRQ9#*) is shared with *ISA_IRQ9* and both are assigned to the IRQ9 level in the interrupt controller.
- The interrupt from PCI slot2 *(IRQ11#*) is shared with *ISA_IRQ11* and both are assigned to the IRQ11 level in the interrupt controller.

5.2 PowerPC 601 System Implementation Using the ZB

The ZB part adds four level-sensitive PCI inputs that can be steered to any unused ISA IRQ level. In addition, the ZB adds level and edge sensitivity that is selectable on an interrupt-by-interrupt basis (versus on a bank-by-bank basis on the IB). With the SIO ZB part, PCI interrupts from the PCI slots can be routed to two of the four PCI interrupt request inputs `(PIRQ[3:0]#`). The interrupts from PCI slot1 (old *IRQ9#*) should be wired to `PIRQ1#,` while the interrupts from PCI slot2 (old *IRQ11#*) should be wired to `PIRQ0#`. The remaining `PIRQ2#` and `PIRQ3#` inputs are not used. In addition, the ZB should be programmed such that both `PIRQ0#` and `PIRQ1#` are routed (internally to the chip) to the IRQ15 level in the interrupt controller. (PCI interrupts from the PCI slots are no longer shared with ISA interrupts on IRQ9 and IRQ11. All PCI interrupts from the PCI slots are assigned to IRQ15. IRQ15 is not used by the ISA devices.) To route the `PIRQ0#` and `PIRQ1#` interrupts to IRQ15, the ZB registers shown in NO TAG must be set. NO TAG illustrates the PCI interrupt implementation using the ZB.

Pin 41 `(IRQ15`) of the ZB should not be used for ISA interrupts and should be tied to GND, and the *IRQ15* line on the riser or board riser connector should be tied low in order to prevent any ISA devices from using this interrupt line.

The dot-ORing of the four PCI interrupts (A,B,C,D) of each PCI slot into a single interrupt should remain unchanged from current PowerPC 601 evaluation board implementation.

Pins 68 and 43 on the I/O EPLD become no-connects. Wire IRQ9 (pin 184 in the ZB) and IRQ11 (pin 37) to the ISA slots.

In the ZB, the LTIM bit (bit 3 of ISA ports 0020h and 00A0h) is not used by the interrupt controller and is always read as 1b.

The edge/level select bit for IRQ13 (bit 5 of the INT CNTRL 2 register at 04D1h) must always be set to 0b (edge sensitive).

Each PCI slot (ABCD) should be connected to a separate PIRQx input as shown. This allows software flexibility to route the PIRQs to different interrupt levels if required in the future.

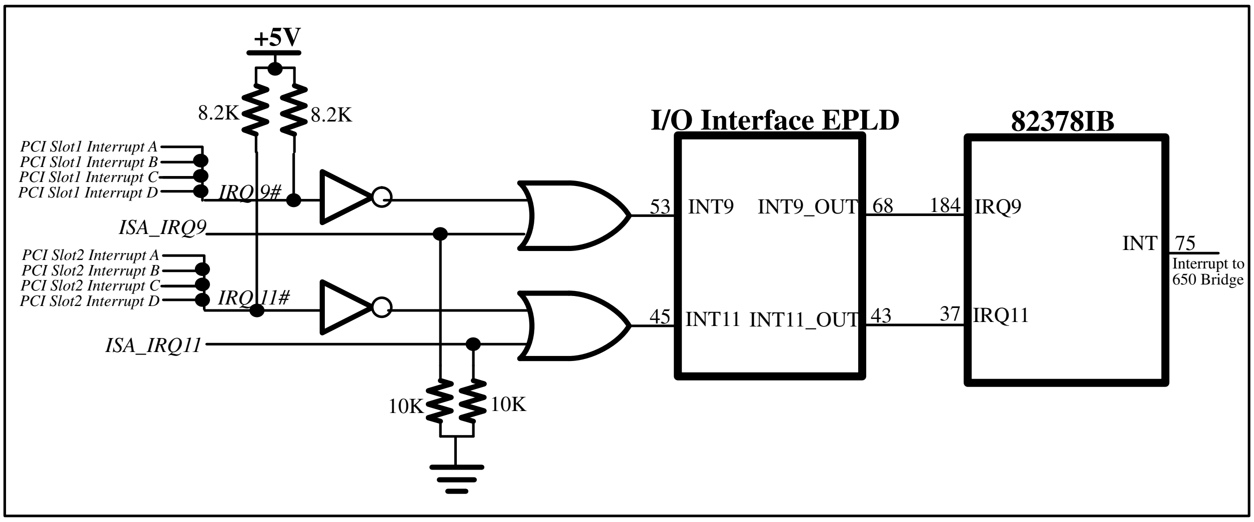

Figure 1. Implementation of PCI Interrupts Using the IB

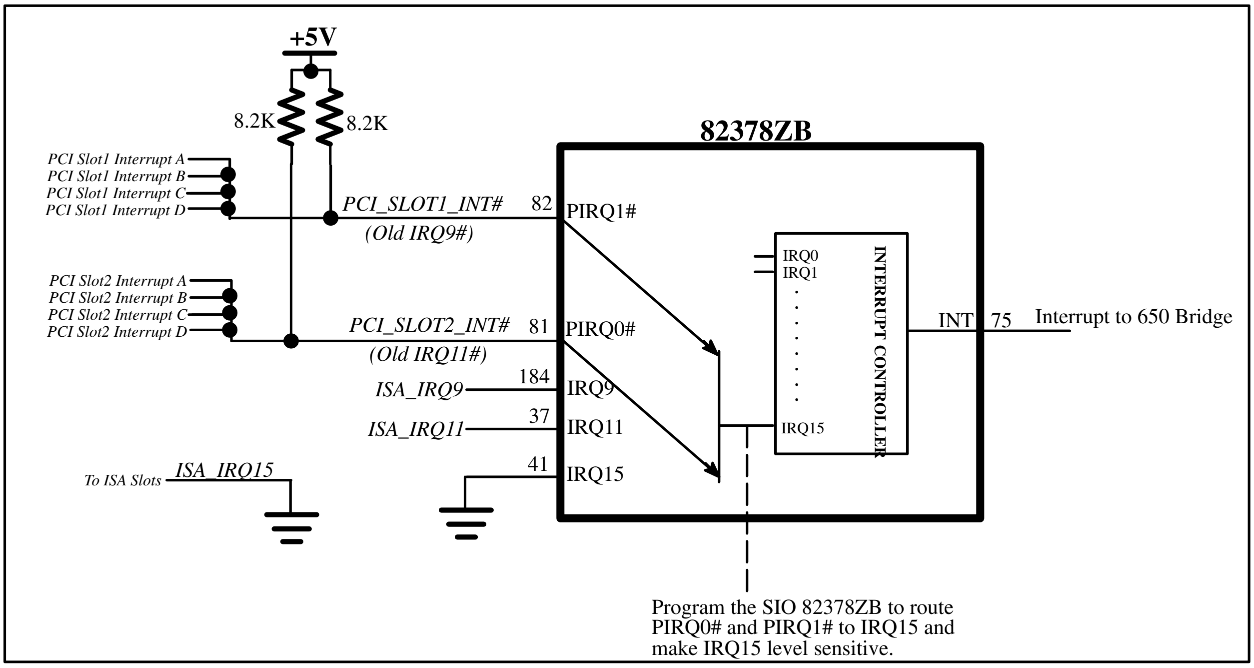

Figure 2. Implementation of PCI Interrupts Using the ZB

Table 2. ZB Register Settings

Register Name	Address (Hex)	Bits	Value to be Set	Default Value	Description
PIRQ0 Route Control Register	8080 0860h	7:0	0Fh	80h	Routes `PIRQ0#` interrupts to IRQ15 level
PIRQ1 Route Control Register	8080 0861h	7:0	0Fh	80h	Routes `PIRQ1#` interrupts to IRQ15 level
INT CNTRL2 Edge/Level Control Register	8000 04D1h	7	0b	1b	Sets IRQ15 to level sensitive

6 Ports 0838h and 083Ch

In the 601 evaluation board, I/O ports 0838h and 083Ch were used to convert the PCI interrupt to edge sensitive. These ports are no longer used and they do not need to be supported in software or hardware. Accessing these ports has no effect on the hardware if IRQ9 and IRQ11 are not connected to the EPLD.

7 IB Errata

The following features are functional on the ZB:

- Scatter/Gather
- GAT mode
- DMA line buffer

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